format. The conversion process generates a conversion matrix from the data structure. The conversion matrix represents the behavior of the circuit element in a generic format. The conversion process then determines a generic HDL register and a plurality of generic HDL input logic for the generic HDL register to replicate the behavior represented by the data structure based on the conversion matrix.

IN THE SPECIFICATION

Please replace the following paragraphs:

The paragraph at Page 12, Line 12 to Page 13, Line 2:

For instance, referring back to Figure 1, the UDP table defines $N = 3$ inputs and one output. Expanding the UDP out to a conversion matrix will result in a 3^4 by 3^4 (81 by 81) conversion matrix. For example, line 1 of the UDP table can be expanded out to three lines in the UDP table for the three possible values represented by "?" in the Q column. The state of line 1 for D, CLK, SET, and Q can be written as a set of four bits. For instance, the current state for line 1 of D = 1, CLK = 0, SET = 0, and Q = ? could be written as 100?. Expanding the question mark out, the three lines would be 1001, 1000, and 100X. Each line is an "edge" line in that an edge transition is defined in the line for the CLK input to transition from 0 to 1, called a rising or positive edge. In which case, the next states for each respective line in the table would be 1101. Since each line in the

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